This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1(currently amended). A semiconductor package, comprising:

a substrate having an upper surface and a lower surface opposed to the upper surface;

a semiconductor chip having an active surface, a back surface opposed to the active surface and a plurality of bonding pads formed on the active surface;

a plurality of conductive devices, the conductive devices formed on the bonding pads and electrically connecting the active surface of the semiconductor chip and the upper surface of the substrate; [[and]]

a thermal enhance layer formed on the back surface of the semiconductor chip,

wherein the substrate has an opening and the semiconductor chip is disposed in the opening; and

an encapsulant encapsulating the semiconductor chip and the conductive device and exposing the thermal enhance layer .

2(canceled).

3(original). The semiconductor package of claim 1, wherein a material of the thermal enhance layer comprises thermally conductive polymer layer.

4(original). The semiconductor package of claim 3, wherein a material of the thermally conductive polymer layer comprises thermally conductive film.

5(original). The semiconductor package of claim 3, wherein a material of the thermally conductive polymer layer comprises thermally conductive epoxy.

6 - 16 (canceled).

17(original). The semiconductor package of claim 1, further comprising a plurality of solder balls formed on the lower surface of the substrate.

Claims 18-27(canceled).

28(new). A semiconductor package, comprising:

a substrate having an upper surface and a lower surface opposed to the upper surface;

a first semiconductor chip attached on the upper surface of the substrate, the first semiconductor chip having a first active surface, a first back surface opposed to the first active surface and a plurality of first bonding pads formed on the first active surface;

a second semiconductor chip attached on the lower surface of the substrate, the second semiconductor chip having a second active surface, a second back surface opposed to the second active surface and a plurality of second bonding pads formed on the second active surface;

a plurality of first conductive bumps formed on the first bonding pads and electrically connecting the first active surface of the first semiconductor chip and the upper surface of the substrate;

a plurality of second conductive bumps formed on the second bonding pads and electrically connecting the second active surface of the second semiconductor chip and the lower surface of the substrate; and

a thermal enhance layer formed on the back surfaces of the first semiconductor chip.

29(new). The semiconductor package of claim 28, further comprising underfills disposed between the first active surface of the first semiconductor chip and the upper

surface of the substrate, and disposed between the second active surface of the second semiconductor chip and the lower surface of the substrate.

30(new). The semiconductor package of claim 28, wherein a material of the thermal enhance layer comprises thermally conductive polymer layer.

31(new). The semiconductor package of claim 30, wherein a material of the thermally conductive polymer layer comprises thermally conductive film.

32(new). The semiconductor package of claim 30, wherein a material of the thermally conductive polymer layer comprises thermally conductive epoxy.

33(new). The semiconductor package of claim 28, wherein the active surface of the semiconductor chip faces and connects to the upper surface of the substrate via the conductive bumps.

34(new). The semiconductor package of claim 28, further comprising a plurality of solder balls formed on the lower surface of the substrate.

35(new). A semiconductor package, comprising:

a substrate having an upper surface and a lower surface opposed to the upper surface;

a first semiconductor chip attached on the upper surface of the substrate, the first semiconductor chip having a first active surface, a first back surface opposed to the first active surface and a plurality of first bonding pads formed on the first active surface;

a second semiconductor chip attached on the lower surface of the substrate, the second semiconductor chip having a second active surface, a second back surface

opposed to the second active surface and a plurality of second bonding pads formed on the second active surface;

a plurality of first conductive devices, the first conductive devices formed on the bonding pads and electrically connecting the first active surface of the first semiconductor chip and the upper surface of the substrate;

a thermal enhance layer formed on the first back surface of the first semiconductor chip; and

a plurality of solder balls formed on the lower surface of the substrate.

36(new). The semiconductor package of claim 35, further comprising underfills disposed between the first active surface of the first semiconductor chip and the upper surface co the substrate, and disposed between the second active surface of the second semiconductor chip and the lower surface of the substrate.

37(new). The semiconductor package of claim 35, wherein a material of the thermal enhance layer comprises thermally conductive polymer layer.

38(new). The semiconductor package of claim 37, wherein a material of the thermally conductive polymer layer comprises thermally conductive film.

39(new). The semiconductor package of claim 37, wherein a material of the thermally conductive polymer layer comprises thermally conductive epoxy.

40(new). The semiconductor package of claim 35, further comprising a plurality of second conductive devices, the second conductive devices formed on the bonding pads and electrically connecting the second active surface of the second semiconductor chip and the lower surface of the substrate.

41(new). The semiconductor package of claim 35, wherein the first conductive devices are conductive bumps, and the first active surface of the first semiconductor chip faces and connects to the upper surface of the substrate via the conductive bumps.

42(new). The semiconductor package of claim 35, wherein the first conductive devices are conductive wires, and the back surface of the first semiconductor chip faces and connects to the upper surface of the substrate via the thermal enhance layer.

43(new). The semiconductor package of claim 40, wherein the second conductive devices are conductive bumps, and the second active surface of the second semiconductor chip faces and connects to the lower surface of the substrate via the conductive bumps.

44(new). The semiconductor package of claim 40, wherein the second conductive devices are conductive wires, and the back surface of the second semiconductor chip faces and connects to the lower surface of the substrate via the